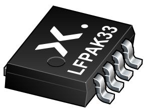

PSMN6R5-30MLD

N-channel 30 V, 6.5 mΩ logic level MOSFET in LFPAK33 using NextPowerS3 Technology

5 July 2017 Product data sheet

1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK33 package. NextPowerS3 portfolio utilising NXP's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETS with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

2. Features and benefits

- Ultra low Q_G, Q_{GD} and Q_{OSS} for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor > 1
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with < 1 µA leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Mini Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Exposed leads for optimal visual solder inspection

3. Applications

- On-board DC-to-DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	30	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	65	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	51	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 15 A; T_j = 25 °C; Fig. 10		-	7	8.6	mΩ

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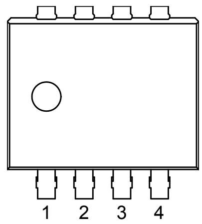
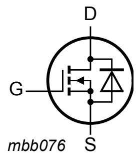
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 15 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	1.7	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK33 (SOT1210)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN6R5-30MLD	LFPAK33	Plastic single ended surface mounted package (LFPAK33); 8 leads	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN6R5-30MLD	6D530L

8. Limiting values

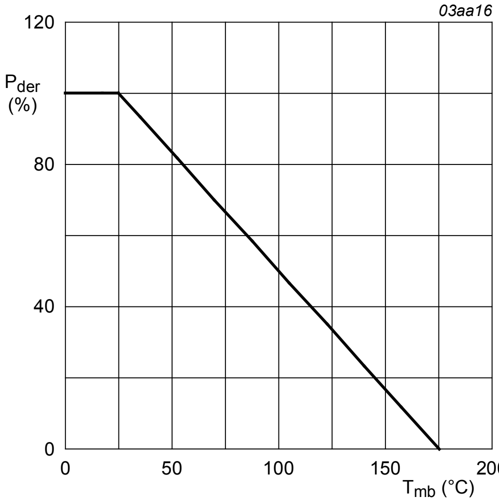
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	30	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	30	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	51	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	65	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	46	A

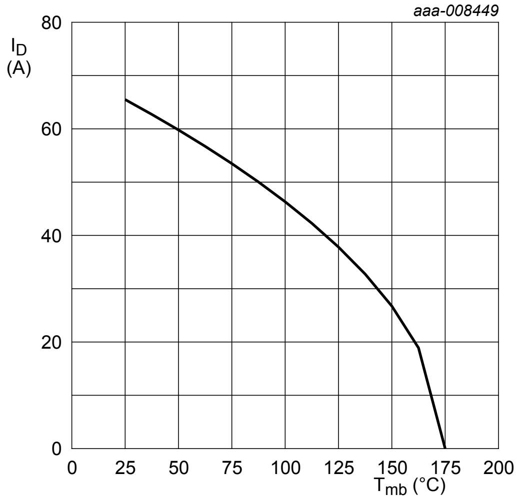
Symbol	Parameter	Conditions		Min	Max	Unit
I_{DM}	peak drain current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C; Fig. 3		-	262	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	42	A
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C		-	262	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 15 A; $V_{sup} \leq$ 30 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 146 µs	[1]	-	42.7	mJ

[1] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10 V$

Fig. 2. Continuous drain current as a function of mounting base temperature

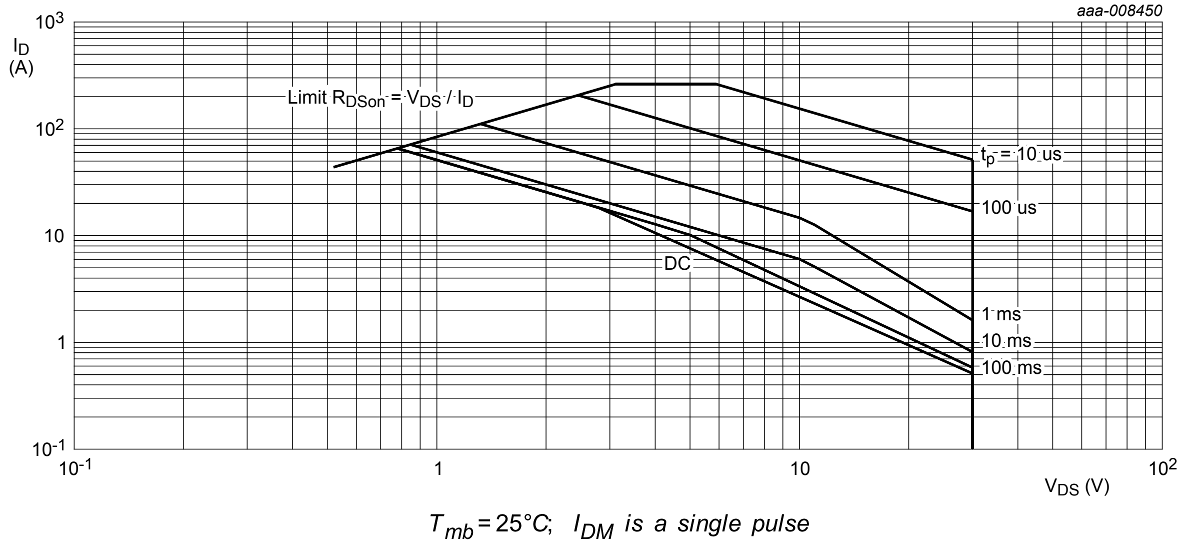


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	2.72	2.94	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5		-	57	-	K/W
		Fig. 6		-	178	-	K/W

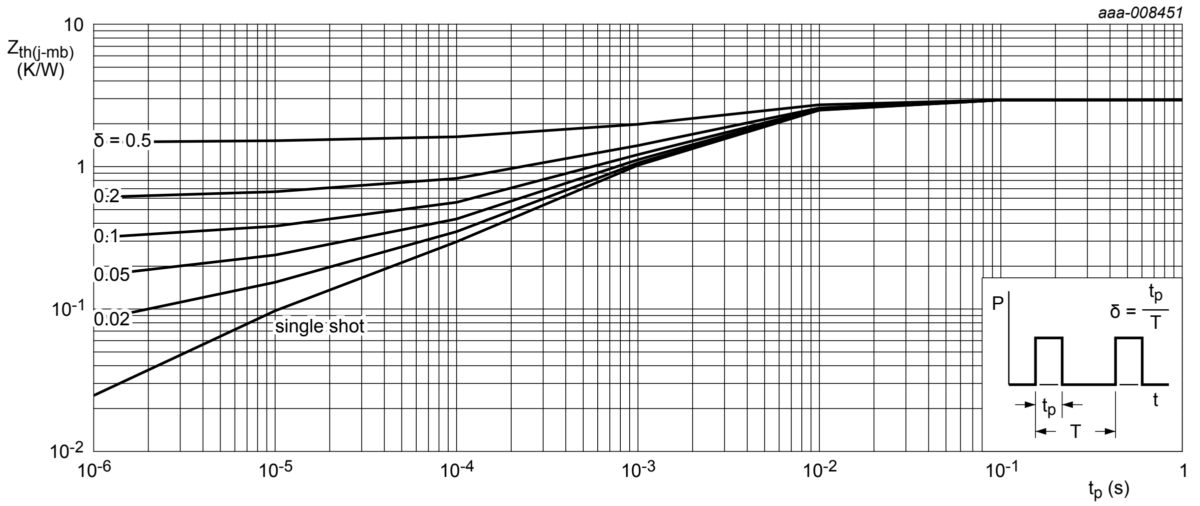


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

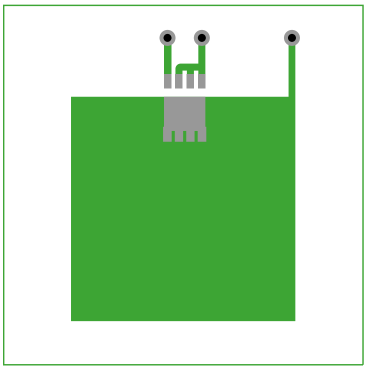


Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

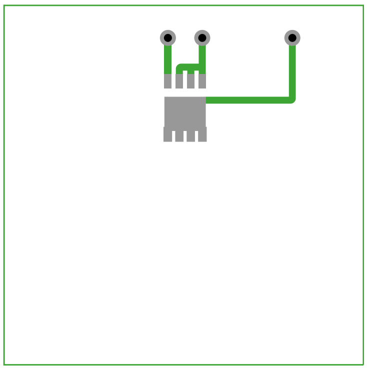


Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		1.2	1.68	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	-3.9	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 24 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 24 V; V_{GS} = 0 V; T_j = 125 °C		-	0.42	-	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 15 A; T_j = 25 °C; Fig. 10		-	7	8.6	mΩ
		V_{GS} = 4.5 V; I_D = 15 A; T_j = 150 °C; Fig. 10; Fig. 11		-	-	14.2	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C; Fig. 10		-	5.5	6.5	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 150 °C; Fig. 10; Fig. 11		-	-	10.7	mΩ
R_G	gate resistance	f = 1 MHz		-	0.44	-	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 15 A; V_{DS} = 15 V; V_{GS} = 10 V; Fig. 12; Fig. 13		-	13.6	-	nC
		I_D = 15 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	6.4	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	12.7	-	nC
Q_{GS}	gate-source charge	I_D = 15 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 12; Fig. 13		-	1.5	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	1.3	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	0.2	-	nC
Q_{GD}	gate-drain charge			-	1.7	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 15 A; V_{DS} = 15 V; Fig. 12; Fig. 13		-	2	-	V
C_{iss}	input capacitance	V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 14		-	817	-	pF
C_{oss}	output capacitance			-	605	-	pF
C_{rss}	reverse transfer capacitance			-	62	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 1 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5 Ω		-	7.5	-	ns
t_r	rise time			-	11	-	ns
$t_{d(off)}$	turn-off delay time			-	9.8	-	ns
t_f	fall time			-	7.2	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 15 V; f = 1 MHz; T_j = 25 °C		-	12.3	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 10 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15		-	0.81	1.2	V
t_{rr}	reverse recovery time	I_S = 15 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 15 V; Fig. 16		-	23.8	-	ns
Q_r	recovered charge		[1]	-	12.6	-	nC
t_a	reverse recovery rise time			-	10.3	-	ns
t_b	reverse recovery fall time			-	13.5	-	ns
S	softness factor			-	1.3	-	

[1] includes capacitive recovery

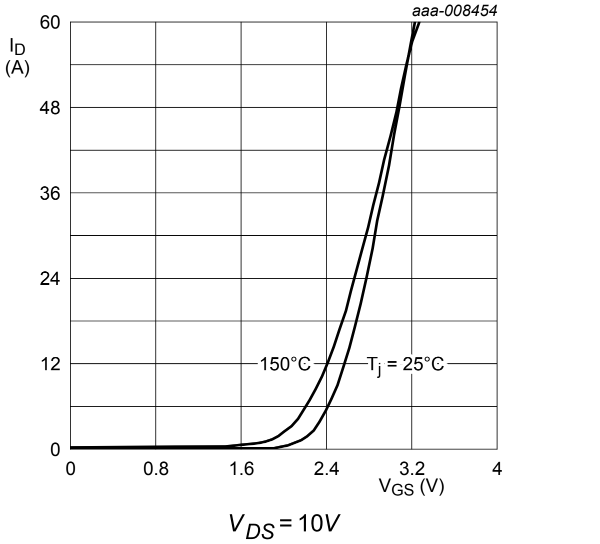


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

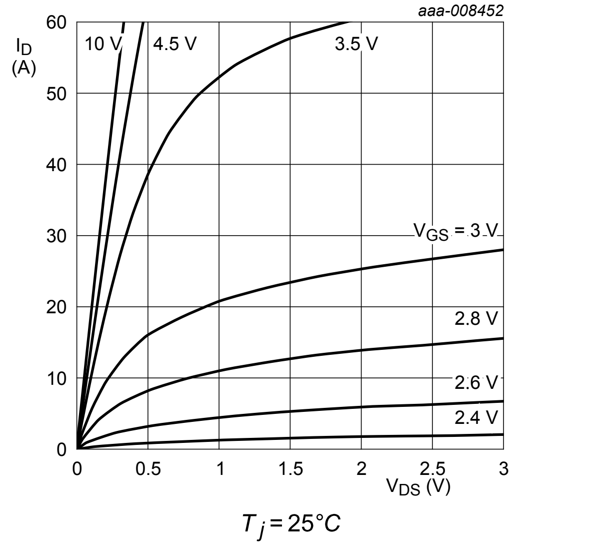


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

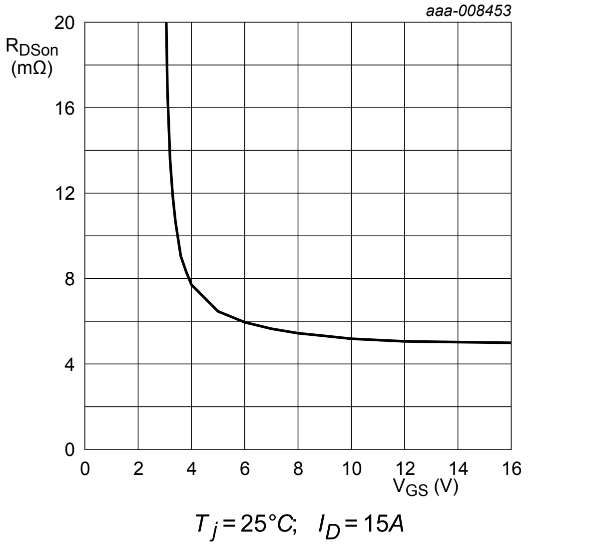


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

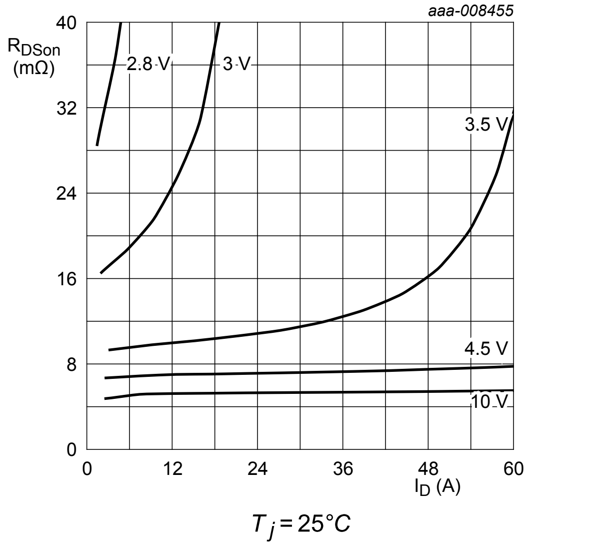
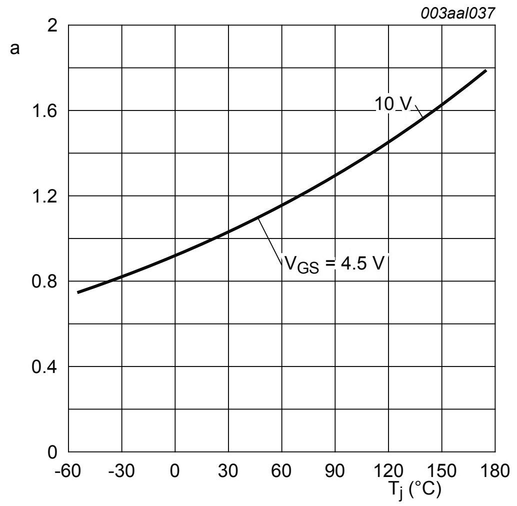


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}\,(25°C)}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

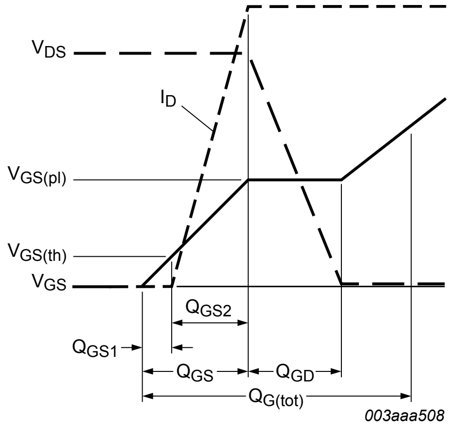
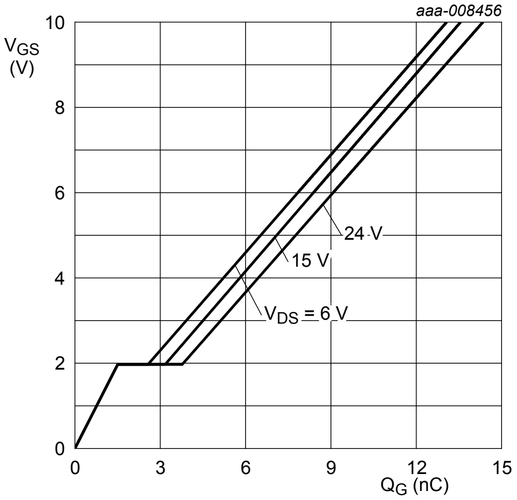
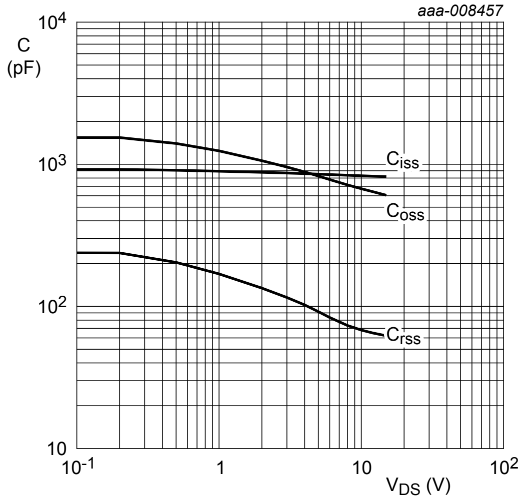


Fig. 12. Gate charge waveform definitions



$T_j = 25°C;\quad I_D = 15A$

Fig. 13. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V;\quad f = 1MHz$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

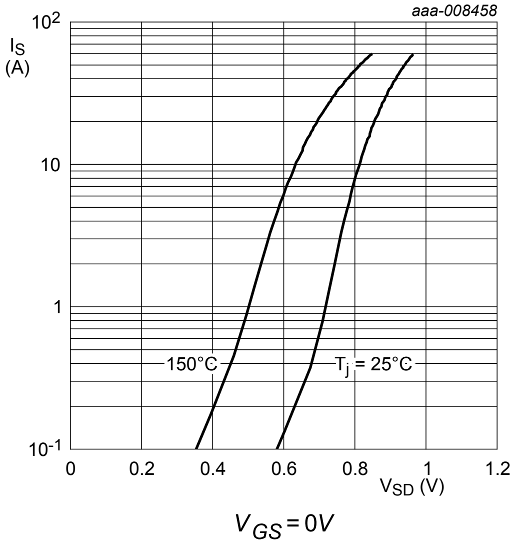


Fig. 15. Source current as a function of source-drain voltage; typical values

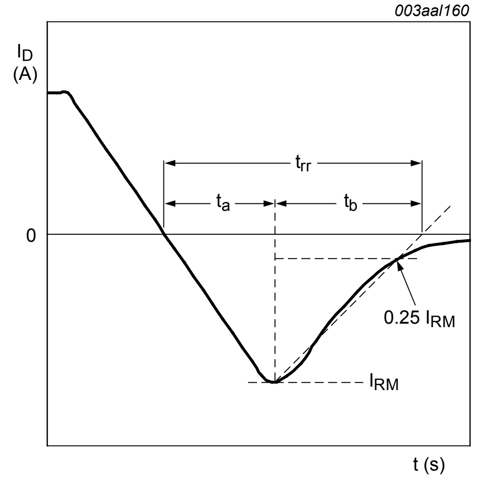
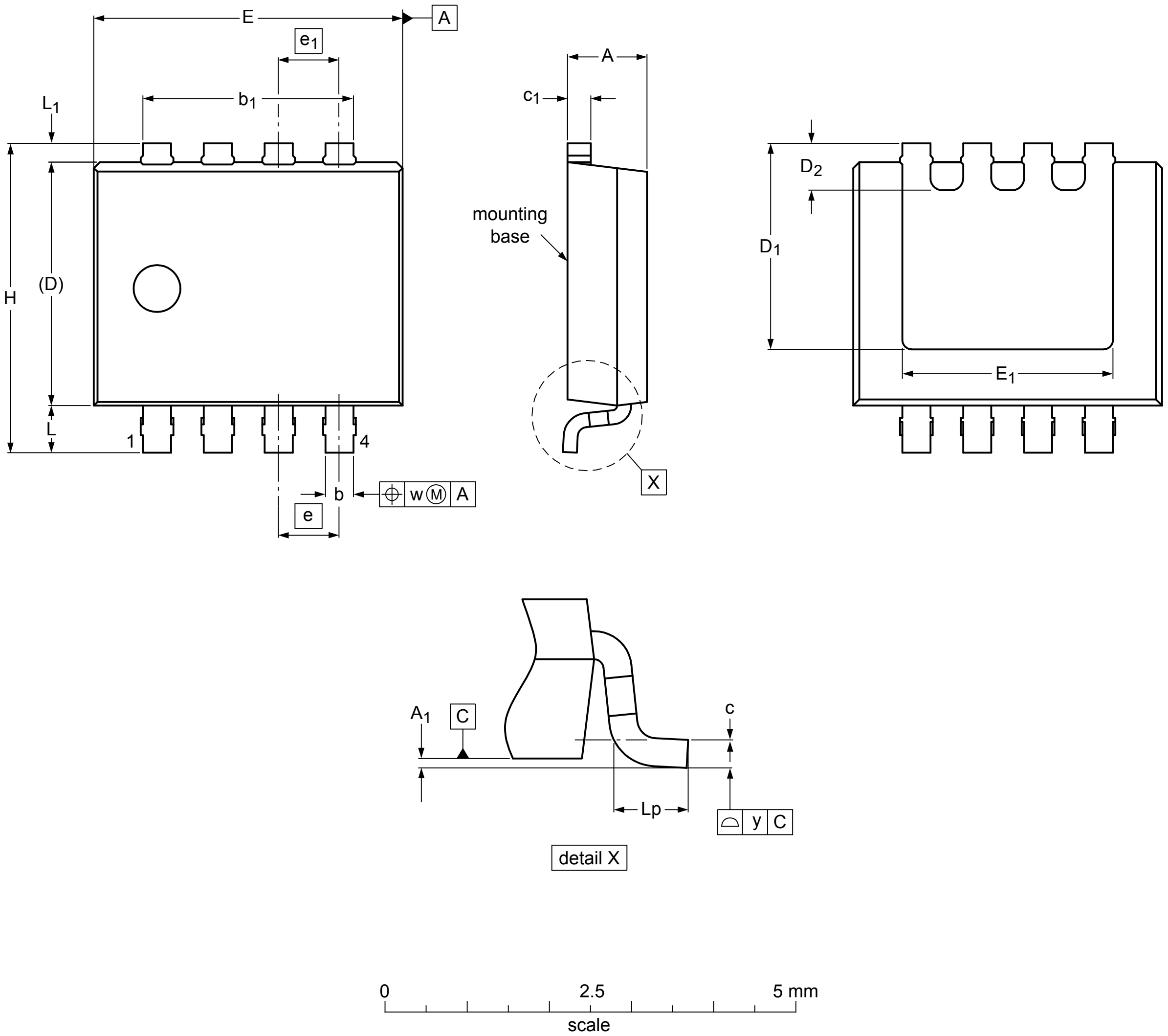


Fig. 16. Reverse recovery timing definition

11. Package outline

Plastic single ended surface mounted package (LFPAK33); 8 leads **SOT1210**



Dimensions

Unit[(1)]		A	A_1	b[(1)]	b_1[(1)]	c	c_1	D ref	D_1	D_2	E[(1)]	E_1	e	e_1	H	L	L_1	L_p	w	y
mm	max	0.90	0.10	0.35	2.4	0.20	0.30		2.35		3.40	2.45			3.40	0.65	0.25	0.50		
	nom							2.60		0.50			0.65	0.65					0.20	0.10
	min	0.80	0.00	0.25	2.2	0.10	0.20		1.90		3.20	2.00			3.20	0.45	0.13	0.30		

Note

1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1210_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1210						~~14-04-25~~ 16-08-09

Fig. 17. Package outline LFPAK33 (SOT1210)

12. Soldering

Footprint information for reflow soldering of LFPAK33 package **SOT1210**

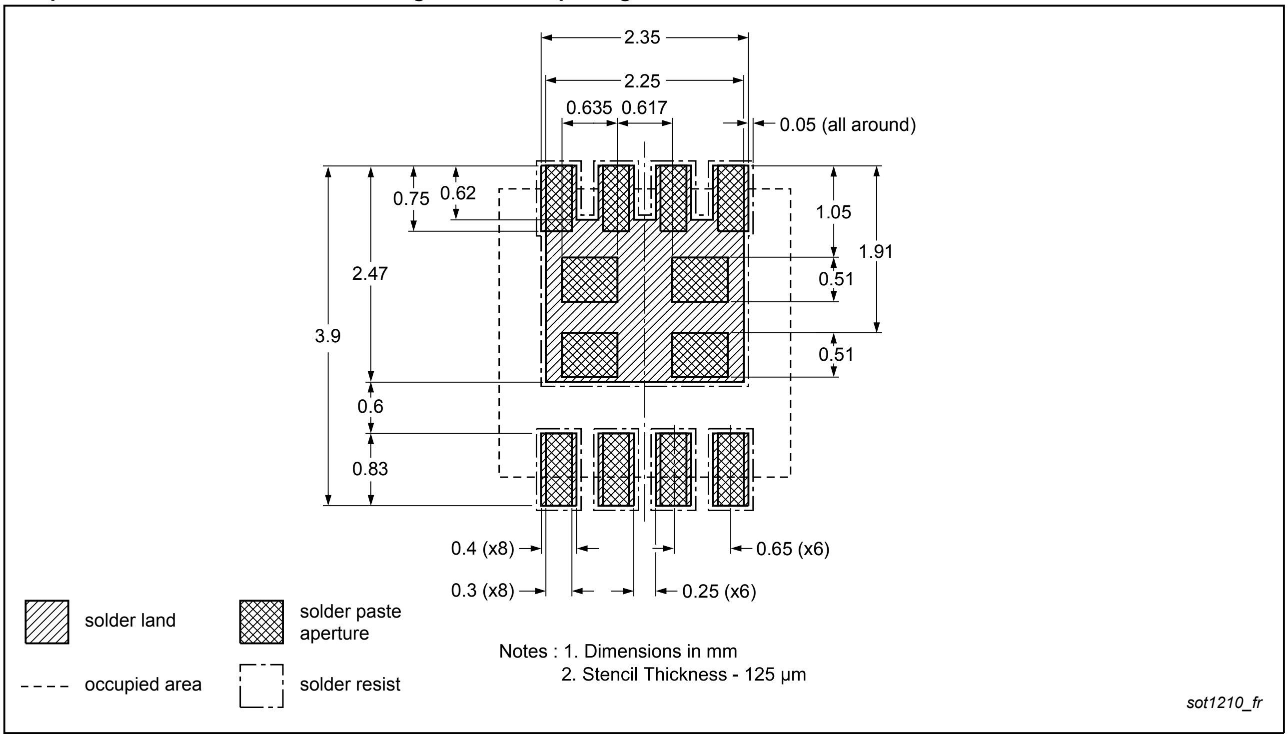


Fig. 18. Reflow soldering footprint for LFPAK33 (SOT1210)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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14. Contents

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Date of release: 5 July 2017